DRIVE TECHNIQUES FOR HIGH SIDE N-CHANNEL MOSFETs

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Drive Techniques for High Side N-Channel MOSFETs

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Although upper half-bridge N-channels are inevitably more difficult to drive than their P-channel complements, a variety of relatively simple straightforward circuits are described that can do the job. Bootstrapping or charge pumping provide the above-rail bias that is required, and a variety of common inexpensive components provide level shifting and drive.

As power MOSFET technology has matured, the advantages of using N-channel MOSFETs for power control have steadily become more pronounced. Fourth generation MOSFETs take this trend a big step further. In addition to on-resistance improvements, fourth generation devices feature Drain-Source diodes that have both the speed and ruggedness to match MOSFET performance in bridge circuits. The power control characteristics of these devices are so much better than P-channel and PNP alternatives, that it is highly desirable to use N-channel MOSFETs for both upper and lower half positions in low voltage bridges.

Although driving upper half-bridge N-channel MOSFETs is usually more complex than using P-channel complements, relatively straightforward and economical circuits can do the job. A collection of these circuits is presented in the following discussion. Bias voltage, drivers, and level shift techniques are considered. In many situations, these techniques save considerably more in power device costs than what is spent on increased drive complexity.

Providing Bias Voltage

The essential issue in driving upper half-bridge N-channels is developing a gate bias voltage that exceeds the power rail. This requirement is illustrated in *Figure 1*, where a 12V bias supply ties to the power rail and provides bias power for high side drivers. There are several ways to provide this type of bias. In situations where you have control over power supply design, an extra floating power supply output is conceptually the most straightforward way to provide bias voltage. As shown in *Figure 2*, the additional winding is referenced to the power rail, and configured to provide a DC voltage that exceeds the rail by roughly 12 to 15V.

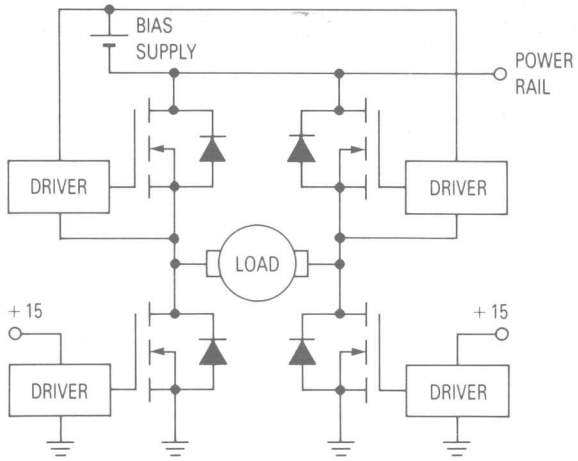


Figure 1. Bias Voltage

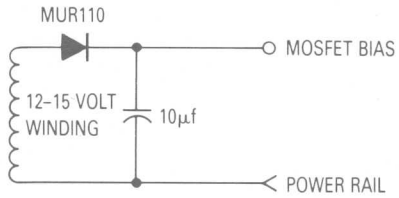


Figure 2. Power Supply Winding

Although this technique is conceptually simple, the power supply winding can be expensive and unattractive for a variety of reasons. An inexpensive alternative is shown in *Figure 3*. This circuit is a charge pump based upon the 555 timer. It is simple, inexpensive, and easily provides the few milliamps of average bias current that is required for driving high side N-channel MOSFETs.

Operation is very similar to a voltage doubler, except that output capacitor C2 is referenced to the power rail rather than the 555's supply voltage. In a straightforward manner, R_T and C_T configure the 555 as a 35kHz oscillator. As the 555's output switches approximately

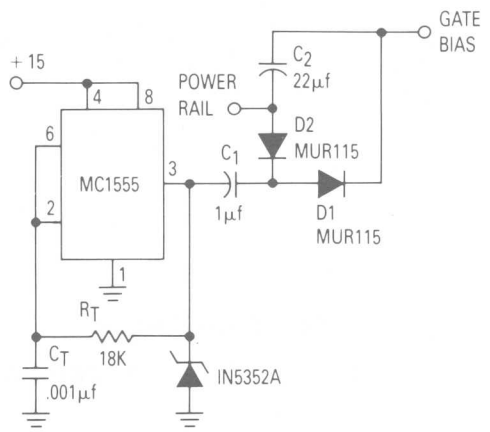


Figure 3. 555 Charge Pump

from ground to its supply voltage, charge is transferred from C1 to C2 through forward biased diode, D1. In the other direction, as the 555 goes from high to low, D1 reverse biases, D2 forward biases and C1's charge is replenished from the power rail. On a repetitive basis the voltage developed across C2 approximates the 555's supply voltage, provided that average output current is relatively small. With the values shown, up to 10mA of bias current can be supplied and still produce 12V above the power rail for high side drivers. The zener on pin 3 does not affect normal operation. However, it is required to ensure the 555's survival as the power rail voltage is initially applied to C1.

For switching power supplies and Brushless DC motors, another alternative to an additional power supply output is bootstrapping. In its simplest form, bootstrapping is illustrated in the buck converter shown in *Figure 4*. As power is initially applied to this circuit the load voltage starts out at zero. Therefore, a path is provided from V_{in} through D1, L1 and the load to charge reservoir capacitor C_R to very nearly the input voltage. Once C_R has been charged, D1 will back bias and allow the high side of C_R to float above V_{in} when Q1 is turned on. Because a relatively small amount of charge is depleted from C_R while Q1 remains on, a relatively stable bias voltage is maintained.

As Q1 is turned off, its source goes roughly a diode drop below ground, which forward biases D1 and replenishes the charge on C_R. This happens each switching cycle on a repetitive basis and maintains the voltage across C_R. The same type of technique can be used in half- and full-bridge power supplies. It is also well suited to Brushless DC motor drives where commutation of the motor provides a similar automatic refreshing of reservoir capacitors. However, this technique is not well suited to brush type motor drives where an upper half-bridge transistor can be on continuously and complex refresh schemes are needed to make bootstrapping work.

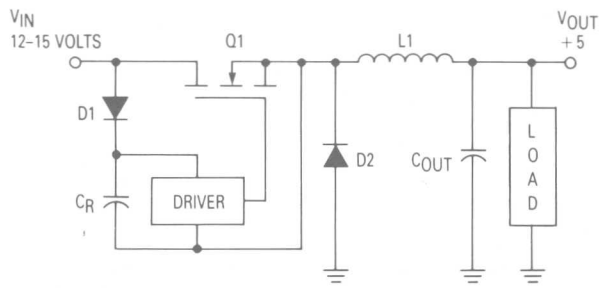


Figure 4. Bootstrap Technique

An example of how bootstrapping is used in a Brushless DC motor drive appears in *Figure 5*. In this circuit an MC33034 control IC is shown driving one phase of a three-phase output bridge. Operation is very similar to the buck converter. Initially as power is brought up, motor voltage is zero and reservoir capacitor C_R charges through the MC33034's +15V supply until Q5 is turned on. When Q5 is switched on the voltage at Phase A rises, D1 back biases, and the MPSW01 / MPSW51 drive pair receives a bias from C_R that floats above the power rail. As the motor rotates and Q6 becomes turned on, the voltage at Phase A approaches ground, D1 again becomes forward biased, and C_R is automatically recharged from the +15V supply. This technique is best suited to applications such as fans, blowers, and disk drives where charge depletion during a motor stall is not normally a problem. However, refresh

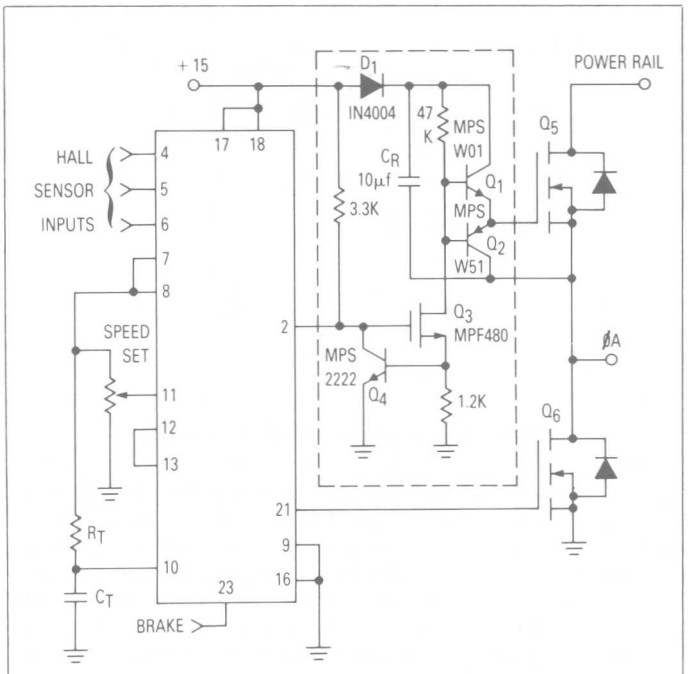


Figure 5. Bootstrapped Brushless Motor Output Stage

during a stall can be accomplished quite easily when an MC33034 is used as the control IC. It has a brake feature that turns on all three lower outputs and turns off all three upper outputs. This condition returns motor voltage to ground, hence momentary application of a brake signal provides refreshing of bootstrap capacitors.

Driver Design

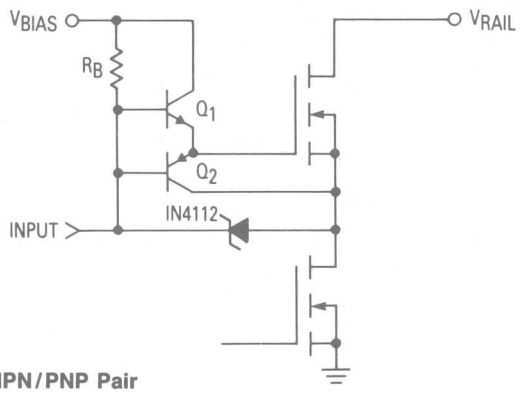
When either a charge pump or bootstrapping is used to provide bias power, driver designs that require a minimum amount of average bias current are an important consideration. In order to facilitate level shifting, it is also desirable for high side drivers to accept inputs that are either ground-referenced current sinks or optically-generated. Three drives that meet these requirements are illustrated in *Figure 6*. Of these, the NPN / PNP voltage follower in *Figure 6a* is the most generally applicable. It is simple, low cost, and works well with inexpensive TO-92 transistors.

For this kind of driver there are significantly different design constraints depending upon how V_{BIAS} is generated. If V_{BIAS} is generated from bootstrapping, then both Q1 and Q2 can be low voltage devices that have to withstand voltages no greater than the maximum value of V_{BIAS}. In bootstrapped designs, the gate protection zener can also be eliminated since maximum gate voltage does not exceed V_{BIAS}. On the other hand, when V_{BIAS} is referenced to the power rail, driver requirements are more stringent. In this case maximum available drive voltage is V_{RAIL} + V_{BIAS}, and the zener is required to keep gate-source voltage within acceptable limits. Since V_{BIAS} + V_{RAIL} can also appear across the collector-base junction of Q1, a voltage rating in excess of the peak power rail voltage is required. For higher voltage rails, the MPSA42-A45 series is a good choice. These devices provide voltage ratings up to 400V in TO-92 packages.

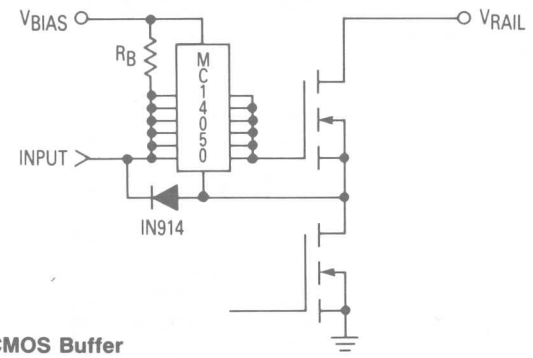
A CMOS buffer can be substituted for discrete transistors, and is shown in *Figure 6b*. As shown, this circuit is restricted to applications where V_{BIAS} is referenced to the upper MOSFET's source, due to the IC's

18V breakdown limitation. Therefore, it is suitable for bootstrapped designs, but not situations where a charge pump or power supply winding are tied to the power rail. Since the CMOS buffer has a quiescent current requirement that is measured in microamperes, and a high input impedance, this type of driver can be used to minimize the rate at which charge is depleted from bootstrap capacitors. Of the three circuits shown, this one allows the highest values of R_B. It, therefore, provides the longest holdup time for a given size bootstrap capacitor and minimum power dissipation in level shifting circuitry.

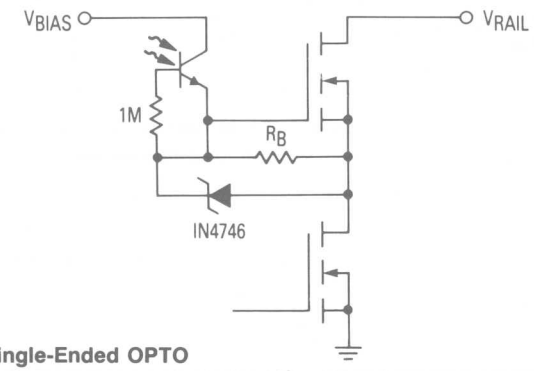
When level shifting is taken into account the OPTO driver in *Figure 6c* minimizes parts count. As shown, it is too slow for the majority of PWM applications, but is well-suited to motor bridges where upper half devices are used for direction or commutation but not PWM. This circuit has considerations similar to the NPN / PNP pair in *Figure 6a*. If V_{BIAS} is derived from bootstrapping, the OPTO transistor can be a low voltage type and the 1N4746 zener is not



6a. NPN/PNP Pair

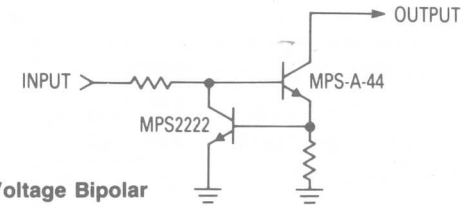


6b. CMOS Buffer

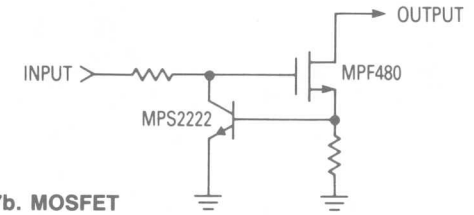


6c. Single-Ended OPTO

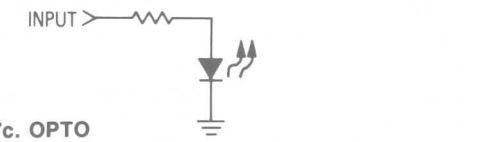
Figure 6. Drive Circuits



7a. High Voltage Bipolar



7b. MOSFET



7c. OPTO

Figure 7. Level Translation

needed. However, if V_{BIAS} is derived from a charge pump or a power supply winding that is referenced to the power rail, the zener is required and the OPTO transistor's voltage rating must exceed $V_{BIAS} + V_{RAIL}$. For requirements up to 400V the MOC8204 does the job.

Level Translation

With all of the foregoing drivers, leveling shifting is quite efficient since the amount of current that has to flow through the power rail voltage is generally less than 1mA. Key design requirements are sink current, saturation voltage, breakdown voltage, and switching speed. The amount of sink current required is determined by the values chosen for R_B in *Figures 6a* and *6b*. As a minimum, the level translator has to sink enough current to swing R_B through V_{BIAS}. An effective method for doing this is shown in *Figures 7a* and *7b*. These configurations provide a semi-regulated sink current and allow the current sink's saturation voltage to easily make a 1V spec at room temperature.

Saturation voltage is especially important when the driver in *Figure 6a* is used. With this circuit a maximum saturation voltage of approximately 1V is required to keep both upper and lower half-bridge transistors from simultaneous conduction. Referring again to *Figure 5*, if the lower half-bridge is turned on then level shifting transistor Q3 will be on also. In this state the voltage at Q3's drain plus a base-emitter drop at Q2 determines the upper half-bridge transistor's maximum gate voltage. At small load currents the voltage drop across Q6 can approach zero. Therefore,the level shifter's saturation voltage plus a base-emitter drop should not exceed Q5's minimum threshold spec of 1.5V.

The choice of transistors in *Figures 7a* and *7b* represents a tradeoff between speed and breakdown voltage. With an MPS-A44 level shift transistor, the bipolar version in *Figure 7a* supports power rail voltages that approach 400V. However, transistion times for the MPS-A44 typically run 4 to 5 μsec. Where higher speeds are required, MPF480 or MPF481 TMOS TO-92s in the configuration of *Figure 7b*

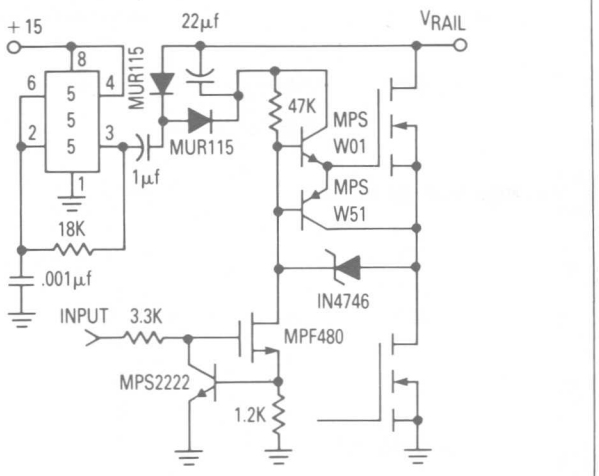


Figure 8a. Charge Pump/Discrete/FET

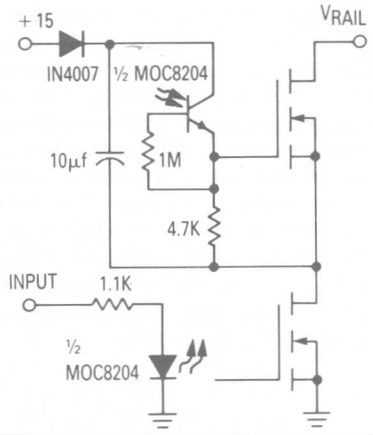


Figure 8b. Bootstrap/OPTO

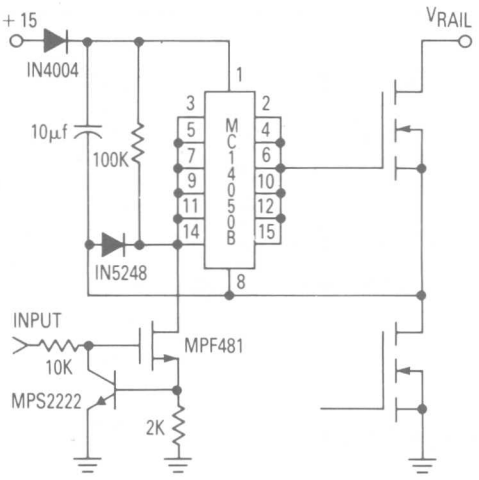


Figure 8c. Bootstrap/CMOS/FET

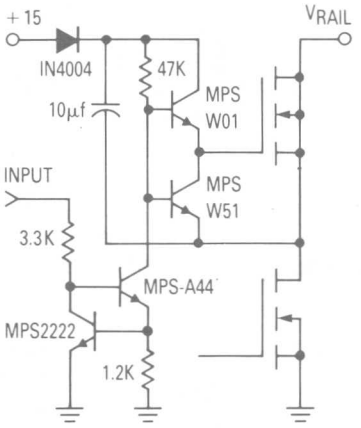


Figure 8d. Bootstrap/Discrete/Bipolar

are a better choice. The tradeoff here is voltage. Assuming 15V for V_{BIAS}, the maximum peak rail voltage that can be accommodated with an MPF481 is 165V.

Mix and Match

The bias, drive, and level shifting techniques that have been discussed so far can be combined in a variety of ways. Of 27 possible combinations, the four that make the most sense are shown in *Figure 8* with all the pieces tied together. In *Figure 8a*, a charge pump is used in combination with a discrete driver and MOSFET level shifter. This combination is well suited to low voltage brush motors where the top half-bridge may be on continuously. The simplest combination appears in *Figure 8b* where OPTO isolation and drive are combined with a bootstrapped bias supply. This one is best suited for commutating Brushless DC motors, and is unique among the four in that it will work with 1000V output devices. If minimum level shift current and high speed are design objectives, the combination in *Figure 8c* provides some interesting characteristics. With 250µA of level shift current, this circuit switches an MTP3055E in 50nsec. For off-line Brushless DC motors, the combination in *Figure 8d* provides 400V of level shift capability with a simple straightforward circuit.

Comparative Results

Whichever one of the high side N-channel drives is used, component cost is quite favorable compared to a P-channel / N-channel complementary approach. Even at the lower end of the power spectrum, lower power device costs more than offset the cost of additional drive components. For example, if component costs for the complementary output stage in *Figure 9* are compared to costs for the output stage in *Figure 8c*, the numbers in Table 1 can be generated. These costs are based upon 100-piece distributor prices for semiconductors and capacitors, and 2500-piece prices for resistors. They are also based upon relatively small 12-15A / 60V power devices, the MPT12P06 and MTP3055E.

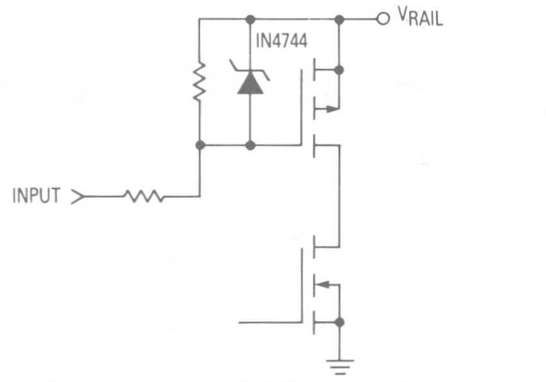


Figure 9. Complementary Output Stage

Even at the relatively modest power level that is reflected in Table 1, component costs for the all N-channel output stage are roughly 20% lower. As power levels go up, driver costs remain constant and total component cost becomes dominated by the cost differential between P-channel and N-channel power MOSFETs. Therefore, all N-channel configurations become increasingly attractive as power levels go up.

Table 1

Cost Comparison

All N-Channel (Figure 8c)		Complementary (Figure 9)	
Component	Price ($)	Component	Price ($)
1N4004	0.15	1N4744	0.45
MC14050BCP	0.42	2 Resistors	0.06
MPF481	0.28	MTP12P06	2.60
MPS2222	0.09	MPT3055E	0.57
10μF Cap.	0.55		3.68
3 Resistors	0.09		
1N5248A	0.14		
MTP3055E	0.57		
MTP3055E	0.57		
	2.86		

Acknowledgements

1. To Jade Alberkrack for the 555 Charge Pump circuit.
2. To Jim Hagerman for the Buck Regulator Bootstrapping technique.

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